1. A memory cell, comprising gated lateral bipolar transistors and having bistable current states for storing information, one of said current states being achieved by operation of gate-induced latchup of said transistors.

2. The memory cell of claim 1 wherein said gated lateral bipolar transistors comprise two complementary vertical bipolar transistors.

3. The memory cell of claim 2 wherein said complementary bipolar transistors comprise a p-n-p transistor and an n-p-n transistor and the collector region of said p-n-p transistor is connected with the base region of said n-p-n transistor.

4. The memory cell of claim 3 wherein said p-n-p transistor further comprises a gate in connection with the n-region of said transistor.

5. The memory cell of claim 4 wherein said n-p-n transistor further comprises a gate in connection with the p-region of said transistor.

6. The memory cell of claim 5 wherein said gate-induced latchup is achieved by a pulsed gate bias.

7. The memory cell of claim 6 wherein said pulsed gate bias biases the gate in connection with one of the n-region or the p-region and subsequently biases the gate in connection with the other of the n-region or p-region.

8. The memory cell of claim 1 wherein said cell is a static random access memory cell.

9. The memory cell of claim 1 wherein said cell has an area of about $4F^2$ where F is the minimum lithographic dimension.

10. A circuit for storing information as one of at least two possible bistable current states, comprising

at least one vertical p-n-p-n structure containing a bipolar p-n-p transistor merged with a bipolar n-p-n transistor;

a transistor gate in connection with the n-region of said p-n-p transistor; and

a transistor gate in connection with the p-region of said n-p-n transistor.

11. The circuit of claim 10 wherein said transistor gates operate to latch-up said p-n-p-n structure and said latch-up results in one of said bistable current states.

12. The memory cell of claim 11 wherein said pulsed gate bias biases the gate in connection with one of the n-region or the p-region and subsequently biases the gate in connection with the other of the n-region or p-region.

13. The circuit of claim 11 further comprising a substrate for supporting said vertical p-n-p-n structure.

14. The circuit of claim 12 wherein said vertical p-n-p-n structure is disposed in a trench within said substrate.

15. The circuit of claim 11 wherein said circuit is a static random access memory cell.

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16. The circuit of claim 14 wherein said memory cell has an area of about $4F^2$ where F is the minimum lithographic dimension.

17. A SRAM cell, comprising:

a p-n-p-n transistor having a first p-region, a first n-region, a second p-region, and a second n-region; and

a first gate in connection with the first n-region, and a second gate in connection with said second p-region, wherein said gates are connected to at least one voltage source for producing latch-up in said p-n-p-n transistor as one of the bistable current states for storing information in said SRAM cell.

18. The SRAM cell of claim 17 wherein said latch-up is produced by providing a pulsed gate bias.

19. The memory cell of claim 18 wherein said pulsed gate bias biases the gate in connection with one of the first n-region or the second p-region and subsequently biases the gate in connection with the other of the first n-region or second p-region.

20. The SRAM cell of claim 17 further comprising a substrate for supporting said p-n-p-n transistor and wherein said p-n-p-n transistor is a vertical structure disposed within a trench in said substrate.

21. The SRAM cell of claim 17 further comprising a row address line in connection with the first p-region and a column address line in connection with the second n-region.

22. The SRAM cell of claim 21 further comprising a write row address line in connection with said gate connecting to said first n-region, and a column write address line in connection with said gate connecting to said second p-region.

23. A SRAM array, comprising

a substrate;

a plurality of vertical p-n-p-n transistors;

a first set of isolation trenches between said p-n-p-n transistors for isolating said transistors in a first direction;

a second set of isolation trenches orthogonal to said first set of trenches for isolating said transistors in a second direction;

a gate line in at least some of said trenches of said first set of trenches and connecting the n-regions of at least some of said plurality of transistors; and

a gate line in at least some of said trenches of said second set of trenches and connecting the p-regions of at least some of said plurality of transistors.

24. The SRAM array of claim 23 further comprising an insulating material layer between each of said p-n-p-n transistors and the substrate, horizontally isolating the transistors.

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25. The SRAM array of claim 24 wherein said insulating material is an oxide.

26. The SRAM array of claim 24 wherein said insulating material is a buried n-type layer.

27. The SRAM array of claim 23 wherein said plurality of p-n-p-n transistors are inverted transistors and are supported on a p-type substrate.

28. A computer system, comprising

a processor; and

a memory circuit connected to the processor, the memory circuit containing at least one memory cell comprising two gated complementary bipolar transistors and having bistable current states for storing information, one of said current states being achieved by operation of gate-induced latch-up of said transistors, wherein the complementary bipolar transistors comprise a vertical p-n-p transistor and a vertical n-p-n transistor and the collector region of said p-n-p transistor is connected with the base region of said n-p-n transistor.

29. The computer system of claim 33 wherein said p-n-p transistor has a gate in connection with the n-region of said transistor, and said n-p-n transistor has a gate in

connection with the p-region of said transistor.

30. The computer system of claim 28 wherein said gate-induced latchup is achieved by a pulsed gate bias.

31. The computer system of claim 30 wherein said pulsed gate bias biases the gate in connection with one of the n-region or the p-region and subsequently biases the gate in connection with the other of the n-region or p-region.

32. The computer system of claim 28 wherein said memory cell is a static random access memory cell.

33. The computer system of claim 32 wherein said static random access memory cell has an area of about $4F^2$ where F is the minimum lithographic dimension.

34. A method of forming a memory cell for storing information as one of at least two possible bistable current states, the method comprising the following steps:

providing a semiconductor substrate;

providing doped silicon regions in the following doping profile: p, n, p and n, to form a vertical p-n-p-n transistor;

forming a p-type polysilicon gate in connection with the n-region of said transistor; and

forming an n-type polysilicon gate in connection with the p-region of said transistor.

35. The method of claim 34 wherein said substrate is a p-type substrate and said method further comprises the step of forming an insulating material layer between the transistor and the substrate.

36. The method of claim 34 further comprising the steps of:

defining a first set of trenches in said p, n, p, n doped silicon regions to a depth at least sufficient to expose the lowermost buried p-type layer;

defining a second set of trenches orthogonal to said first set of trenches to a depth at least sufficient to expose the lowermost buried p-type layer;

defining a p-type polysilicon gate within said first set of trenches and in connection with the n-region of said doped silicon; and

defining a n-type polysilicon gate within said second set of trenches and in connection with the p-region of said doped silicon.

37. The semiconductor processing method of claim 36 further comprising the following step:

growing a gate oxide layer on at least one sidewall of each trench of said first and second sets of trenches before depositing polysilicon to define said gates.

38. The method of claim 34 wherein said p-n-p-n transistor is inverted.

39. A semiconductor processing method of forming CMOS static access memory within a semiconductor substrate, the method comprising the following steps:

providing a semiconductor substrate;

defining an array trench within said substrate;

providing doped silicon in said trench in the following doping profile: p, n, p and n;

defining a first set of trenches in said doped silicon by directional etching to a depth at least sufficient to expose the buried p-type layer;

defining a second set of trenches orthogonal to said first set of trenches by directional etching to a depth at least sufficient to expose the buried p-type layer;

growing a gate oxide layer on at least one of the sidewalls of each trench of said first and second sets of trenches; and

defining a p-type polysilicon gate within each trench of one of said sets of trenches and in connection with the n-regions of said doped silicon, and an n-type polysilicon gate within each trench of said other set of trenches and in connection with the p-regions of said doped silicon.

40. The semiconductor processing method of claim 39 wherein said step of defining p-type and n-type polysilicon gates comprises the following steps:

depositing a p-type polysilicon layer in the first set of trenches;

removing said p-type polysilicon layer, while leaving remaining polysilicon as p-type gate material on one sidewall of each trench of said first set of trenches;

depositing an n-type polysilicon layer in the second set of trenches; and

removing said n-type polysilicon layer, while leaving remaining polysilicon as n-type gate material on one sidewall of each trench of said second set of trenches.

41. The method of claim 40, further comprising the steps of depositing oxide to fill the trenches of said first and second sets of trenches.

42. The method of claim 39 wherein said substrate is a p-type substrate.

43. The method of claim 42 wherein said doping profile is n, p, n, p and n.

44. The method of claim 42 wherein said doping profile is inverted.

45. The method of claim 42 further comprising the step of undercutting said p-type layer to form an evacuated

region and filling said evacuated region with an insulating material.

46. A semiconductor processing method of forming CMOS static access memory within a semiconductor substrate, the method comprising the following steps:

providing a semiconductor substrate;

defining an array trench within said substrate;

providing doped silicon in said trench in the following doping profile: p, n, p and n;

defining a first set of trenches in said doped silicon by directional etching to a depth at least sufficient to expose the buried p-type layer;

defining a second set of trenches orthogonal to said first set of trenches by directional etching to a depth at least sufficient to expose the buried p-type layer;

growing a gate oxide layer on at least one of the sidewalls of each trench of said first and second sets of trenches;

depositing a p-type polysilicon layer in the first set of trenches;

removing said p-type polysilicon layer, while leaving remaining polysilicon as p-type gate material on one sidewall of each trench of said first set of trenches

and in connection with the n-regions of said doped polysilicon;

depositing an n-type polysilicon layer in the second set of trenches;

removing said n-type polysilicon layer, while leaving remaining polysilicon as n-type gate material on one sidewall of each trench of said second set of trenches and in connection with the p-regions of said doped polysilicon; and

depositing oxide to fill the trenches of said first and second sets of trenches.

47. A method of storing a binary logic value comprising:

inducing latch-up in a gated diode.

48. The method of claim 47 wherein the step of inducing latch-up further comprises application of a pulsed gate bias.

49. The method of claim 48 wherein said pulsed gate bias is approximately one volt.

50. The method of claim 47 wherein the step of inducing latch-up further comprises inducement of carrier multiplication and breakdown in the gated diode.

51. The method of claim 47 wherein the step of inducing latch-up further comprises application of a negative voltage.

52. The method of claim 51 wherein said negative voltage is approximately one volt.

53. A method of forming a circuit for storing information as one of at least two possible stable current states, the method comprising the following steps:

providing a semiconductor substrate;

providing doped silicon regions to form a multi-region vertical thyristor having at least four regions;

forming at least two polysilicon gates in connection with at least two separate junctions of said multi-region vertical thyristor; and

connecting said at least two polysilicon gates to a voltage source for producing latch-up in said multi-region vertical thyristor.

54. The method of claim 53 wherein said step of providing doped silicon regions further comprises forming one memory cell.